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Operating Principle of Neutral-Point-Less (NPL) Multilevel Inverter Topology: X-type Inverter

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***Abstract*-Multilevel inverters (MLIs) have gained popularity due to the emerging medium and high-power drive applications such as heavy-duty electric vehicles, electric aircraft, and urban air mobility. A neutral-point-clamped, cascade H-Bridge and flying capacitors are the potential candidates for these applications, but these conventional MLIs have either stacked or floating capacitors causing voltage unbalancing and drifting issues in variable-speed operation. In this paper, a new neutral-point-less (NPL) MLI topology is proposed, which requires neither stacked nor floating capacitors, topologically addressing the voltage balancing and drifting issues. The new NPL MLI topology, namely X-type inverter, reduces the required capacitance and volume of the dc-link capacitor by over 75% compared to that of the conventional MLI topologies. In addition, the X-type inverter produces two equal and opposite common-mode (CM) voltage waveforms, which cancel out the capacitive leakage current for the minimum CM electromagnetic interference (CM EMI) noise. This paper introduces the new NPL MLI topology and the underlying principle of multilevel operation without stacked or floating capacitors. The simulation results verify the NPL multilevel operation with a single dc-link capacitor and over 50 dBuV CM EMI noise reduction compared to that of the conventional two-level inverter.**

I. INTRODUCTION

Multilevel inverters (MLIs) are drawing more attention for medium and high-power industrial and electrified transportation applications due to their high voltage and high-power operation capabilities at low switching frequency and harmonics. The most widely adopted MLI topologies are the neutral-point-clamped (NPC), T-type, cascaded H-bridge (CHB), and flying capacitor (FC). These inverter topologies have been practically used in high-power grid-connected inverter applications where the fundamental frequency is fixed at 50 or 60 Hz and industrial drives [1].

However, these conventional MLIs have a critical challenge to overcome for variable frequency operation (e.g., industrial drives, electric vehicles, and electric airplanes) due to their stacked dc-link capacitor with neutral point connection (see Fig. 1(a)), causing the capacitor voltage to unbalance from the high neutral current at three times of the fundamental frequency [2], [3]. Several advanced modulation techniques, such as carrier-based pulse width modulation (CBPWM) and discontinuous pulse width modulation, and active voltage balancing circuits have been proposed to mitigate the neutral current [2], [4]-[6]. However, these conventional MLI topologies cannot fundamentally address capacitor unbalanced voltage issues due to the presence of either stacked dc-link capacitors with neutral point connection or floating capacitors [7], [8]. The capacitor voltage unbalance issue prohibits reliable variable frequency operation as it leads to increased modulation complexity and switching frequency [4], [9]-[11], high common-voltage (CM) and current and noise, high total harmonic distortion (THD) at medium and high-power applications [12]-[18].

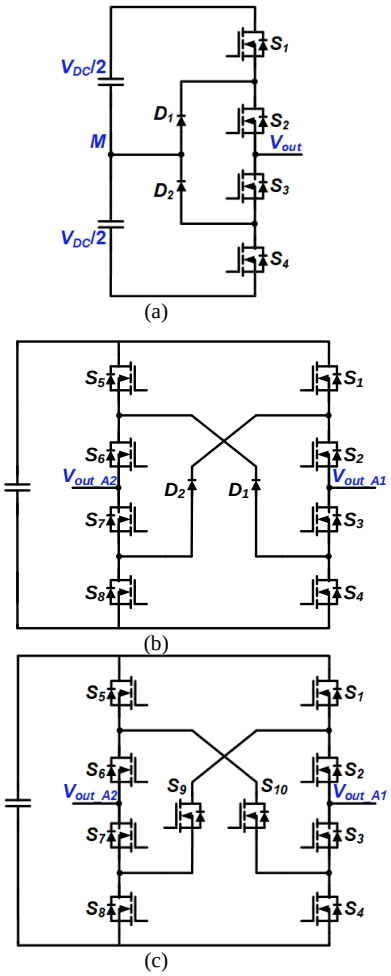


Fig. 1. One phase-leg of (a) conventional NPC; and the proposed X-type topologies with (b) passive interconnection switches; (c) active interconnection switches.

In this paper, a neutral-point-less (NPL) MLI topology called an X-type inverter is proposed and investigated, which can topologically address the capacitor voltage unbalancing issue. The X-type inverter topology does not require either stacked dc-link capacitors or floating capacitors, and one

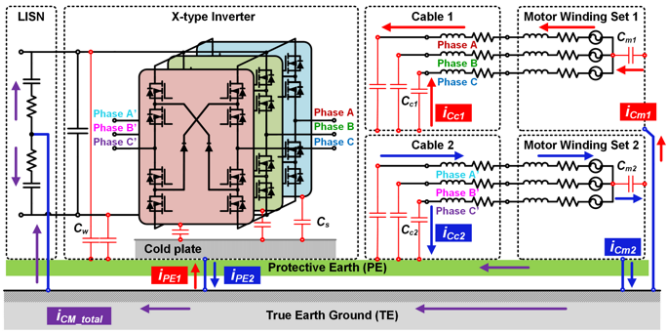


Fig. 2. Full schematic of the proposed X-type inverter with dual motor winding sets (six-phase windings).

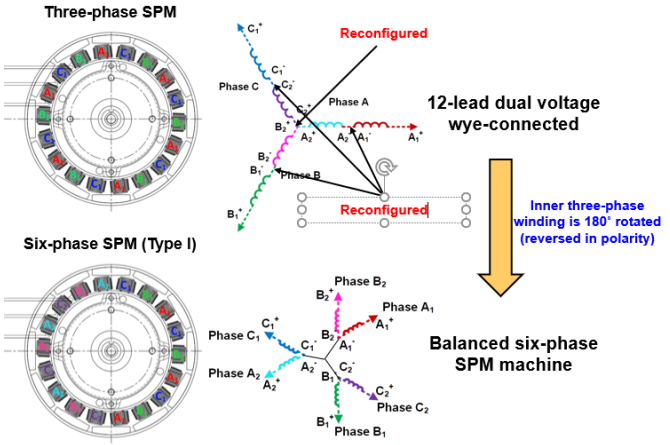


Fig. 3. Electric machine winding reconfiguration for the proposed X-type inverter.

phase-leg is directly interconnected with the opposite phase-leg with a clamping diodes or active switches, illustrated in Fig. 1(b) and (c). The X-type inverter solves the root cause of the dc-link capacitor ripple and unbalances by eliminating the neutral point connection. In addition, it reduces the risks of high and unbalanced voltage stress on the power switches and capacitors leading to improved system reliability and lifespan of the inverter.

The second section of this paper will introduce the new NPL MLI topology, the switch configuration, commutation, and modulation. The third section will demonstrate the X-type inverter operation and CM EMI noise estimation with MATLAB simulation, and the fourth section compares the power and efficiency between the conventional MLI and the X-type inverter. The conclusion is drawn in the last section.

II. NEUTRAL-POINT-LESS MULTILEVEL X-TYPE INVERTER TOPOLOGY

A full schematic of the proposed NPL three-level X-type inverter topology is shown in Fig. 2, which has eight active switching devices and two passive devices per module. Each inverter module produces two equal and opposite three-level output voltages producing total six-phase output voltages without any neutral point connection. The conventional three-phase dual winding electric machines can be easily

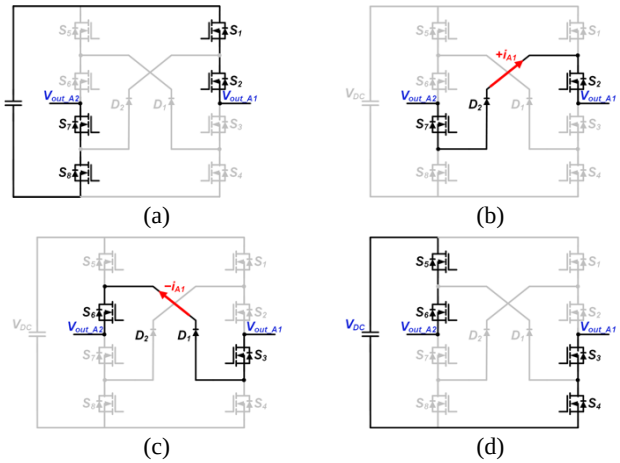


Fig. 4. X-type topology switching states and phase current during the switching operation. (a) positive-negative (PN), (b) ZZ ($+i_{A1}$), (c) ZZ ($-i_{A1}$), and (d) negative-positive (NP).

TABLE I. FOUR SWITCHING STATES OF PROPOSED X-TYPE INVERTER.

State	PN	ZZ ($+i_{A1}$)	ZZ ($-i_{A1}$)	NP
V_{A1}	$+V_{DC}/2$	0	0	$-V_{DC}/2$
V_{A2}	$-V_{DC}/2$	0	0	$+V_{DC}/2$
S_1	on	off	off	off
S_2	on	on	on	off
S_3	off	on	on	on
S_4	off	off	off	on
S_5	off	off	off	on
S_6	off	on	on	on
S_7	on	on	on	off
S_8	on	off	off	off
D_1	off	off	on	off
D_2	off	on	off	Off

reconfigured to be compatible with the proposed X-type inverter, as shown in Fig. 3.

Due to the elimination of the neutral point connection, the X-type inverter provides attractive features such as multilevel operation with a single and small dc-link capacitor, active CM leakage current cancellation for low CM EMI noise, and the balanced and reduced voltage stress on the power switches, and capacitors. Removing the neutral point connection also simplifies a busbar and dc-link capacitor design and reduces the associated parasitic inductances and unnecessary minor power loops. Besides, the X-type inverter has a higher power density than the conventional MLIs, as the elimination of the neutral point leads to over 75% reduction in the dc-link capacitor value and its volume.

A. *Switch Configuration and Switching States*

The passive X-type inverter topology (see Fig. 4) has eight active switches and two passive devices (e.g., Schottky diodes) per one module with two output voltage channels. A complete X-type inverter system requires three modules in total for the dual three-phase operation. The four switching states and output voltages are summarized in Table I. The positive-negative (PN) state is one of the two active switching

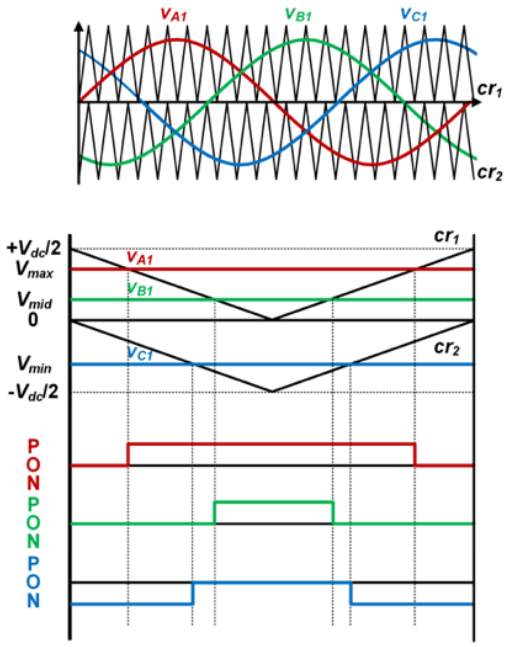


Fig. 5. Multicarrier sine PWM for the proposed X-type inverter.

states where two uppers (S_1/S_2) and two lower switches (S_7/S_8) are on-state to generate positive V_{DC}/2 and negative V_{DC}/2 for each output voltage channel as shown in Fig. 4(a). The negative-positive (NP) state is the other active switching state where two uppers (S_5/S_6) and two lower switches (S_3/S_4) are on to generate negative V_{DC}/2 and positive V_{DC}/2 for each output voltage channel. The two zero switching states of ZZ ($+i_{A1}$) and ZZ ($-i_{A1}$) circulate the equal and opposite phase current between two output voltage channels and generate zero voltage without the neutral point connection to a split dc-link capacitors.

B. *Modulation Techniques*

The X-type inverter has a symmetric structure (two NPC inverters interconnected to each other) and therefore, a simple and conventional multicarrier sine PWM (SPWM) can be utilized as one of the viable modulation techniques. Since the active switch S_1/S_8, S_2/S_7, S_3/S_6, and S_4/S_5 are synchronized and have identical PWM gate signals, the conventional three-phase multicarrier SPWM is used for simulation, as shown in Fig. 5.

III. SIMULATION RESULTS

A full schematic of the proposed X-type inverter is modeled in MATLAB Simulink to validate the multilevel operation capability with a single, not stacked, dc-link capacitor. The X-type inverter is designed to operate with 400 kW output power, 900 V dc-link voltage, 20 kHz switching frequency, and 200 μF dc-link capacitor. It is important to note that the conventional NPC inverter with the same power and voltage rating requires a four to five times higher dc-link capacitance to hold the input voltage stable.

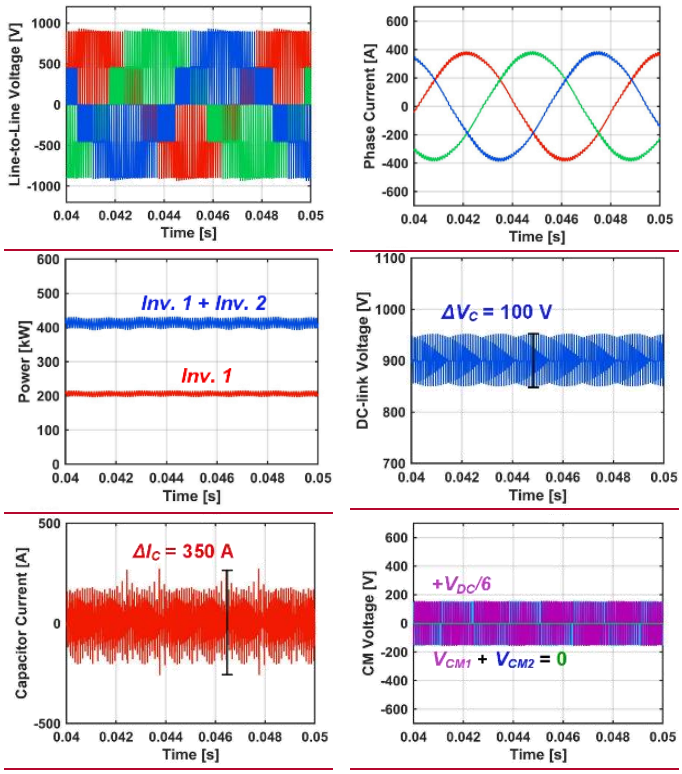


Fig. 6. Simulation results of the X-type inverter (output line-to-line voltage, current, power, dc-link capacitor voltage, current, and CM voltage).

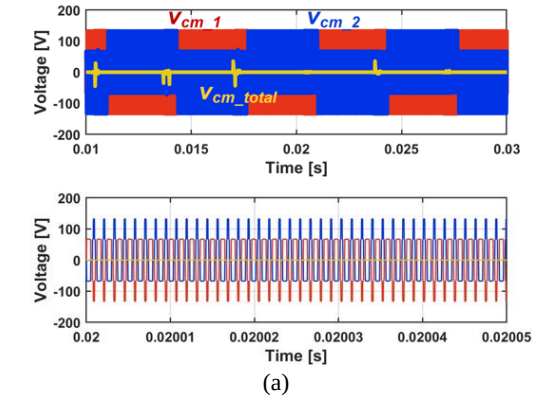
A. *Multilevel Operation with Single dc-link Capacitor*

The line-to-line output voltage waveforms shown in Fig. 6 (top left corner) confirm that the proposed X-type inverter can generate three-level voltage with only a single dc-link capacitor. Accordingly, the output current waveform shows minimal distortion and low harmonics due to multilevel operation. Although there are three more output voltage and current waveforms from the X-type inverter (dual output), only one set of the three-phase waveforms is displayed in Fig. 6 to clearly show the multilevel operation.

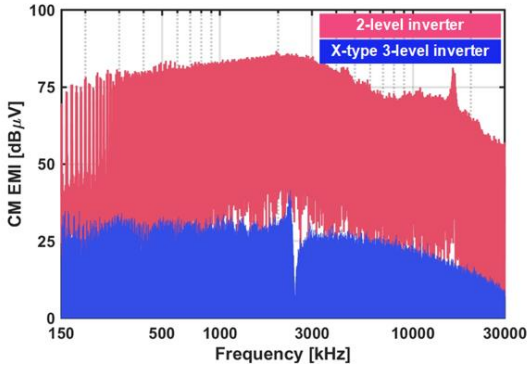
The dual output power waveform is shown in Fig. 6 (middle left corner) where the X-type inverter produces 200 kW from each output and eventually reaches 400 kW in total. It is also critical to mention that the triplen voltage harmonics in the dc-link capacitor are eliminated as shown in Fig. 6 (middle right corner). The dc-link capacitor voltage ripple is only associated with the inverter switching events.

B. *Common-Mode Leakage Current Cancellation*

For CM EMI noise analysis, the X-type inverter is also modeled in the PSIM simulation tool with LISN and spectrum analyzer. The X-type inverter provides active CM leakage current cancellation as shown in Fig. 7(a). The dual output voltage channels produce two equal and opposite CM voltages leading to capacitive leakage current cancellation. The measured CM EMI noise from the conventional two-level inverter is compared with that of the proposed X-type inverter, as shown in Fig. 7(b). The CM EMI spectrum shows



(a)



(b)

Fig. 7. CM EMI simulation results of the X-type inverter. (a) active CM voltage cancellation; (b) CM EMI spectrum comparison between 2-level and proposed X-type 3-level inverter.

that the X-type inverter can reduce the CM EMI noise over 50 dBμV, leading to substantial reduction or even elimination of additional CM filters in the high-voltage and high-power motor drive systems.

IV. Efficiency Analysis and Power Loss Estimation

A. *Estimation of Power Losses*

The passive X-type inverter was modeled in PSIM with 1.2 kV, 24-active (SiC MOSFETs), and 6-passive (SiC diodes) devices. The power distribution of the devices and total power loss have been modeled and analyzed with different output power levels at several switching frequency values for the X-type inverter.

For power loss and efficiency estimation, SiC MOSFET, ROHM-BMS400D12P3G002, and diode thermal model from an IGBT module, NXH350N100H4Q2F2P1G, are used. The SiC device is a half-bridge module, so two modules are series-connected to obtain one phase-leg (active) device configuration for the X-type inverter. Therefore, twelve power modules are required for a three-level X-type inverter design. In addition, for the diodes of the proposed X-type, two diodes are used in parallel to obtain an adequate current limit for full-load operation. Table II summarizes several electrical characteristics of the selected SiC MOSFETs and

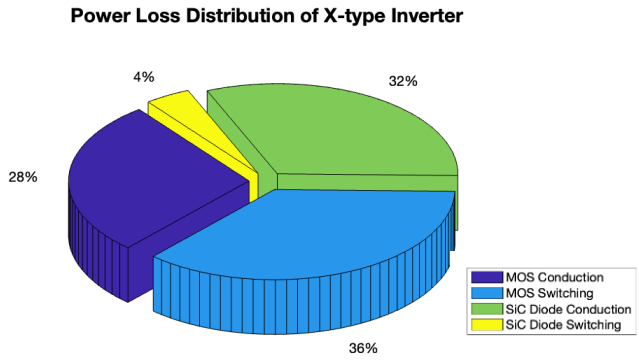


Fig. 8. Power loss distribution of the X-type three-level inverter with 0.92 modulation index at 50 kHz switching frequency.

TABLE II. Selected Device Specifications for X-type Inverter Simulation.

	BV	I_F	V_F	R_{ON}	Op. Temp
SiC MOSFET	1.2 kV	400 A	1.8 – 3 V	6.5 mΩ	-40/175 °C
SiC Diode	1.2 kV	100 A	1.5 – 2 V	4179 nC	-40/175 °C

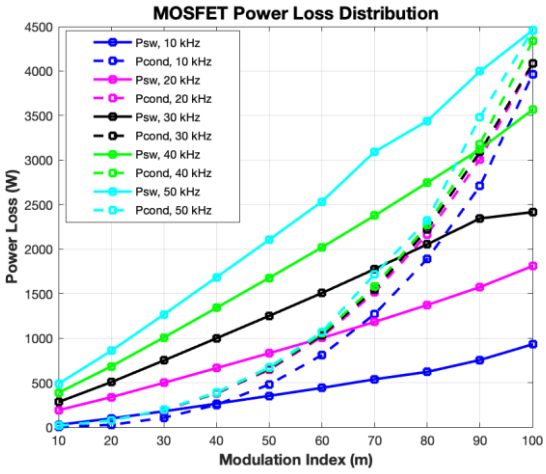
the diodes used in the simulation, which have sufficient voltage and current margins to test the X-type inverter at its maximum power.

A power loss distribution of the proposed X-type topology is drawn in Fig. 8 for 50 kHz switching frequency at 0.92 modulation index. The total input power is 431 kW, and the efficiency of the X-type inverter is 98.15%. The case temperature was fixed at 25 °C during the switching operation. The switching loss of the SiC MOSFETs is dominant in the total loss followed by the diode conduction loss.

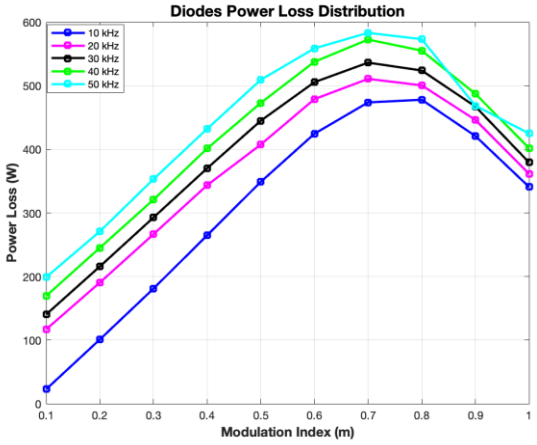
The additional simulation was run at five different switching frequencies (from 10 to 50 kHz) and the full range of the modulation index (from 0.1 to 1). In terms of the power loss distribution for the varying switching frequencies and modulation index, switching and conduction loss of the MOSFET and diode have different characteristics as plotted in Fig. 9(a) and (b). The switching loss of the SiC MOSFET linearly increases while the conduction loss has a parabolic increase as the modulation index increases. In the same manner, diode conduction losses increases linearly with the increased modulation index up to 0.7; however, the switching loss remains low and constant as shown in Fig. 8. It is also important to note that the diode conduction loss increases initially with increasing modulation index due to the increase in the phase current amplitude. However, as the modulation index exceeds 0.7, the conduction loss starts to drop due to the less utilization of zero switching states where the phase current circuiates through the diodes as shown in Fig. 9(b).

B. *Estimation of Inverter System Efficiency*

In order to optimize the power loss distribution of the X-type topology, a set of parametric analysis is conducted at several different modulation indices and switching



(a)



(b)

Fig. 9. Switching and conduction losses vs. modulation index at five different switching frequencies (a) SiC MOSFETs (b) diodes.

frequencies. The power losses of the switching devices are highly dependent on the junction temperature. Therefore, it is critical to consider the variation of the device junction temperature using the device thermal model. The ambient temperature of the SiC MOSFET and diode models has been kept at 25 °C during the switching operation. The set of parametric analyses (i.e., modulation index and switching frequency) for the X-type inverter efficiency is illustrated in Fig. 10. The efficiency range of the proposed configuration is between 84% to 99% regarding switching frequency and modulation index. It is also important to note that the light-load efficiency improves with higher switching frequency due to reduced phase current ripple and the conduction losses.

V. CONCLUSIONS AND FUTURE WORK

In this paper, a novel neutral-point-less multilevel inverter, namely an X-type inverter, is proposed and analyzed in detail to validate its multilevel operation capability with a single, not stacked, dc-link capacitor. The X-type inverter achieved

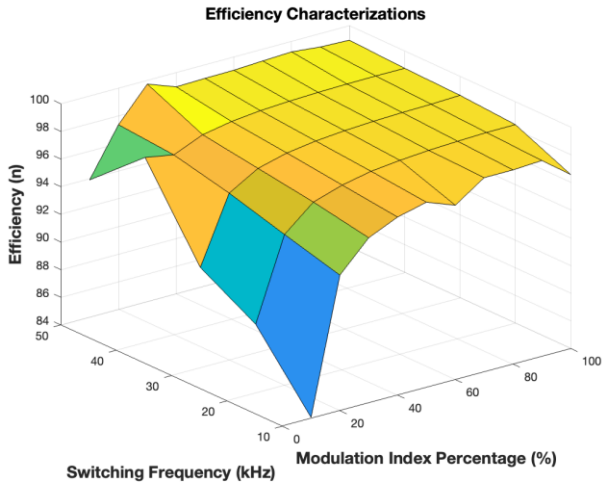


Fig. 10. The efficiency characterization regarding variable modulation index (0.1 to 1) and switching frequency (10 to 50 kHz).

three-level output voltage with a single dc-link capacitor in both MATLAB and PSIM simulations, which leads to over 75% dc-link capacitor size reduction as compared to that of the conventional MLIs. It is also found the X-type inverter produces two equal and opposite CM voltages, which cancel out the capacitive leakage current for a substantial reduction in the CM EMI noise. The simulated CM EMI noise spectrum reveals that the X-type inverter can reduce the CM EMI noise by 50 dBμV in comparison with that of the two-level inverters.

REFERENCES

[1] S. Kouro, J. Rodriguez, Bin Wu, S. Bernet, and M. Perez, "Powering the future of industry: high-power adjustable speed drive topologies," *IEEE Trans. Ind. Appl.*, vol.18, no.4, pp.26-39, July/Aug. 2012.

[2] G. P. Kumar and K. S. Jiji, "Comparison of DC-link Voltage Balancing Strategies for Three Level NPC Inverter," in *2021 International Conference on Intelligent Technologies (CONIT)*, Hubli, India, Jun. 2021, pp. 1–6.

[3] V. Jayakumar, B. Chokkalingam, and J. L. Munda, "A Comprehensive Review on Space Vector Modulation Techniques for Neutral Point Clamped Multi-Level Inverters," *IEEE Access*, vol. 9, pp. 112104–112144, 2021.

[4] X. Lin, S. Gao, J. Li, H. Lei, and Y. Kang, "A new control strategy to balance neutral-point voltage in three-level NPC inverter," in *8th International Conference on Power Electronics - ECCE Asia*, Jeju, Korea (South), May 2011, pp. 2593–2597.

[5] D. Y. Komovskiy, "Comparative analysis of three-level PWM inverters for aircraft AC power systems," in *2016 17th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM)*, Erlagol, Altai Republic, Russia, Jun. 2016, pp. 476–480.

[6] A. Bubert, S. Swain, and R. W. D. Doncker, "Design Considerations of DC-Link Capacitors in NPC Inverters for Electric Vehicles," in *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Chennai, India, Dec. 2018, pp. 1–6.

[7] J. W. Kolar and S. D. Round, “Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems,” *IEE Proc. - Electr. Power Appl.*, vol. 153, no. 4, p. 535, 2006.

[8] Huiqing Wen, Weidong Xiao, Xuhui Wen, and P. Armstrong, “Analysis and Evaluation of DC-Link Capacitors for High-Power-Density Electric Vehicle Drive Systems,” *IEEE Trans. Veh. Technol.*, vol. 61, no. 7, pp. 2950–2964, Sep. 2012.

[9] F. Kieferndorf, M. Basler, L. A. Serpa, J.-H. Fabian, A. Coccia, and G. A. Scheuer, “A new medium voltage drive system based on ANPC-5L technology,” in *2010 IEEE International Conference on Industrial Technology*, Vi a del Mar , Chile, 2010, pp. 643–649.

[10] S.-Jin. Hong, S.-Cheol. Shin, H.-Sung. Kim, and C.-Yuen. Won, “Dead-time compensation and realization method for 3-level NPC Inverter,” in *2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific)*, Beijing, China, Aug. 2014, pp. 1–5.

[11] C. D. New, A. N. Lemmon, B. T. DeBoi, B. W. Nelson, J. Zhao, and A. D. Brovont, “Design and Characterization of a Neutral-Point-Clamped Inverter Using Medium-Voltage Silicon Carbide Power Modules,” in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, Mar. 2020, pp. 2912–2919.

[12] L. Jian, Z. Zhe, Y. Xianggen, and W. Minghao, “FPGA Implementation of a Multi-Level SPWM for Three-Level NPC Inverter,” in *Proceedings of the 41st International Universities Power Engineering Conference*, Newcastle upon Tyne, UK, Sep. 2006, pp. 175–179.

[13] W. Chen and A. Bazzi, “Model-Based Voltage Quality Analysis and Optimization in Post-Fault Reconfigured N-Level NPC Inverter,” *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13706–13715, Dec. 2021.

[14] P. Gaur and P. Singh, “Various control strategies for medium voltage high power multilevel converters: A review,” in *2014 Recent Advances in Engineering and Computational Sciences (RAECS)*, Chandigarh, India, Mar. 2014, pp. 1–6.

[15] P. Qashqai, A. Sheikholeslami, H. Vahedi, and K. Al-Haddad, “A Review on Multilevel Converter Topologies for Electric Transportation Applications,” in *2015 IEEE Vehicle Power and Propulsion Conference (VPPC)*, Montreal, QC, Canada, Oct. 2015, pp. 1–6.

[16] A. S. Maklakov and A. A. Radionov, “EMC evaluation of three level NPC converter based on space vector PWM,” in *2015 IEEE NW Russia Young Researchers in Electrical and Electronic Engineering Conference (EIConRusNW)*, St. Petersburg, Russia, Feb. 2015, pp. 236–240.

[17] M. Schweizer and J. W. Kolar, “Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications,” *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[18] S. Wang, M. Fereydoonian, and W. Lee, “Six-phase three-level neutral point clamped inverter for capacitor voltage balancing and common-mode voltage cancellation,” in *IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2021, pp. 1091-1096.